Selçuk Köse
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Research Interests

- **Research interests:** Very large scale integration (VLSI) systems; On-chip interconnect; Electronic design automation; Power delivery and management; Hardware security; Cryogenic electronics

Work Experience

- **University of Rochester** Rochester, NY
  Chair, Department of Electrical and Computer Engineering *July 2026 - Current*
- **University of Rochester** Rochester, NY
  Professor, Department of Electrical and Computer Engineering *July 2024 - Current*
- **University of Rochester** Rochester, NY
  Associate Professor, Department of Electrical and Computer Engineering *January 2019 - July 2024*
- **University of South Florida** Tampa, FL
  Associate Professor, Department of Electrical Engineering *August 2018 - January 2019*
- **University of South Florida** Tampa, FL
  Assistant Professor, Department of Electrical Engineering *August 2012 - August 2018*
- **University of Rochester** Rochester, NY
  Research Assistant, High Performance Integrated Circuit Design Laboratory *September 2007 - June 2012*
- **Freescale Semiconductor** Tempe, AZ
  Graduate Intern, Microwave and Mixed-Signal Laboratory *May 2010 - August 2010*
- **Eastman Kodak Company** Rochester, NY
  Graduate Intern, CMOS Image Sensors R&D Laboratory *May 2009 - June 2009*
- **Intel Corporation** Santa Clara, CA
  Graduate Intern, Central Technology and Special Circuits Team *Summers of 2007 and 2008*

Education

- **University of Rochester** Rochester, NY
  Doctor of Philosophy in Electrical and Computer Engineering *March 2008 - June 2012*
- **University of Rochester** Rochester, NY
  Master of Science in Electrical and Computer Engineering *September 2006 - March 2008*
- **Bilkent University** Ankara, Turkey
  Bachelor of Science in Electrical and Electronics Engineering *September 2001 - May 2006*

Awards

- USF Faculty Outstanding Research Achievement Award, 2017
  – The most prestigious award for research achievements at USF. Only 17 researchers (out of over 1700 faculty members) received this prestigious university-wide award in 2017
- USF Outstanding Faculty Award, 2016
  – Only 10 researchers (out of over 1700 faculty members) received this prestigious university-wide award in 2016
- Cisco Research Award, 2015, 2016 & 2017

- National Science Foundation CAREER Award, 2014 - (related to distributed on-chip power delivery and control)
  – National Science Foundation's most prestigious award in support of junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education and the integration of education and research within the context of the mission of their organizations
- USF College of Engineering Outstanding Junior Research Achievement Award, 2014
  – Only one assistant professor received this prestigious award in 2014
- Turkiye Is Bankasi *Golden Youth Award* for outstanding success in University Entrance Exam
  – **12**th over 1.5 million candidates, Turkey, 2001
- Full scholarship and stipend awarded by Bilkent University, Ankara, Turkey, 2001-2006
- Awarded with Abroad Undergraduate Education Fellowship by Turkish Government, Turkey, 2001

Sponsored Research

- **Longview Philanthropy - Hardware-Enables Mechanisms (PI Köse)** — $500,000
  On-Chip Voltage Regulators as Analog Sensors for AI Workload Verification — *2026 - 2029*
- **The Center for Emerging and Innovative Sciences (CEIS) (PI Köse)** — $39,905
  Towards Enabling Digital Superconducting Quantum Control — *2026 - 2027*
  *SEEQC covers the fabrication cost of a 4+ SFQ test chips (>$87,000).
- **The Center for Emerging and Innovative Sciences (CEIS) (PI Köse)** — $30,000
  Towards Enabling Digital Superconducting Quantum Control — *2025 - 2026*
  *SEEQC covers the fabrication cost of a 3+ SFQ test chips (>$65,000).
- **National Science Foundation SaTC award (Co-PI Köse)** — $600,000
  Collaborative Research: SaTC: CORE: Small: Exploration of Shared Memory Related Security Challenges in Mobile Computing Platforms — *2024 - 2027*
- **Department of Energy (PI Köse)** — $400,000
  Modeling the Memory-Compute Gap in Large-scale Superconductive Systems — *2023 - 2025*
- **National Science Foundation SHF award (Co-PI Köse)** — $600,000
  SHF: Small: Cryogenic Hybrid Systems Integration Across Multiple Temperature Zones — *2023 - 2026*
- **National Science Foundation FUSE award (Co-PI Köse)** — $333,000
  Atomically Precise Graphene Nanoribbon-based Transistors: Materials, Devices, Circuits, and Systems — *2023 - 2025*
- **Semiconductor Research Corporation LMD award (Co-PI Köse)** — $391,500
  Smarter Nanoelectronics with Atomically Precise Graphene Nanoribbons — *2023 - 2026*
- **Defense Advanced Research Projects Agency (Co-PI Köse)** — $6,068,498
  Highly-Efficient All-to-All Coupled Ising Machines — *2022 - 2027*
- **National Science Foundation Expeditions award (Co-PI Köse)** — $15,000,000
  Expeditions: DISCoVER: Design and Integration of Superconducting Computation for Ventures beyond Exascale Realization — *2022 - 2029*
- **SRC extension of the STARSS award (sole PI Köse)** — $40,000
  SaTC: STARSS: Small: Combined Side-channel Attacks and Mathematical Foundations of Combined Countermeasures — *2020 - 2021*
- **NSF/SRC joint SaTC/STARSS award (sole PI Köse)** — $370,000
  SaTC: STARSS: Small: Combined Side-channel Attacks and Mathematical Foundations of Combined Countermeasures — *2017 - 2021*
- **Cisco Research Award (PI Köse)** — $80,000*
  Reconfigurable Voltage Regulation for Security and Efficiency — *2017 - 2018*
  *Cisco also covers the fabrication cost of a test chip at 28 nm FDSOI technology.

- **I4 Corridor Matching Grant (sole PI Köse)** $50,000
  On-Chip Voltage Regulation in an Advanced Technology *2016 - 2017*
- **Cisco Research Award (PI Köse)** $80,000**
  On-Chip Voltage Regulation in an Advanced Technology *2016 - 2017*
  **Cisco also covers the fabrication cost of a test chip at 28 nm FDSOI technology.
- **Florida Center for Cybersecurity (FC^2) Seed Grant (PI Köse)** $50,000
  Trusted IoT using Cross-layer Leveraging of Reconfigurable Device Signatures *2016 - 2017*
- **Cisco Research Award (sole PI Köse)** $30,000
  On-Chip Voltage Regulation in an Advanced FDSOI Process *2015 - 2016*
- **Florida Center for Cybersecurity (FC^2) Seed Grant (PI Köse)** $50,000
  Aging-Aware Hardware-Trojan Detection at Runtime *2015 - 2016*
- **National Science Foundation CAREER award (sole PI Köse)** $450,000
  CAREER: Regulator-Gating (ReGa): A New On-Chip Power Delivery Architecture *2014 - 2019*

Publications

Books

B1. I. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, **S. Köse**, and E. G. Friedman, *On-Chip Power Delivery and Management, Fourth Edition*, Springer, 2016, ISBN # 978-3319293936.

B2. R. Jakushokas, M. Popovich, A. V. Mezhiba, **S. Köse**, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors, Second Edition*, Springer, 2011, ISBN # 978-1-4419-7870-7.

– Chinese translation by China Machine Press, 2014, Chinese ISBN # 978-7-111-44929-4

Book chapters

BC1. Y. Mustafa and **S. Köse**, *Side-channel Leakage in Suzuki Stack Circuits*, in H. Thapliyal and T. Humble (eds) Quantum Computing - Circuits, Systems, Automation and Applications, Springer 2023, ISBN # .

BC2. T. Jabbari, Y. Mustafa, E. G. Friedman, and **S. Köse**, *Hardware Security of SFQ Circuits*, in R. Topaloglu (ed) Design Automation of Quantum Computers, Springer 2023, ISBN # 978-3-031-15698-4.

BC3. L. Wang, S. Seckiner, and **S. Köse**, *Reliability Enhanced Digital Low-Dropout Regulator with Improved Transient Performance*, in Metzler C., Gaillardon PE., De Micheli G., Silva-Cardenas C., Reis R. (eds) VLSI-SoC: New Technology Enabler. VLSI-SoC 2019. IFIP Advances in Information and Communication Technology, Springer 2020, ISBN # 978-3-030-53273-4.

Journals

J1. A. Y. Salim, S. Seckiner, E. Elmitwalli, Z. Ignjatovic, and **S. Köse**, "A Mixed-Signal SAT Solver for Exploring Nonideal Effects and Scalability in Analog Computation," *IEEE Journal of Solid State Circuits*, under review.

J2. A. Adedokun, Y. Mustafa, and **S. Köse**, "Inductor-free 2ϕ-SQUID Memory with Intrinsic Bistability," *Springer Nature - Computer Science*, under review.

J3. G. Kulzhanova and **S. Köse**, "Side-Channel Attacks on Digital Readout Circuits for Superconducting Qubits," *Quantum Science and Technology*, under review.

J4. Y. Mustafa and **S. Köse**, "Interfacing Superconductor and Semiconductor Digital Electronics," *Applied Physics Reviews*, under review.

J5. Y. Mustafa, B. Peköz, and **S. Köse**, "Reed-Muller Error-Correction Code Encoder for SFQ-to-CMOS Interface Circuits," *IEEE Transactions on Applied Superconductivity*, Vol. 36, No. 5, pp. 1300906, August 2026.

J6. K. Krause, Y. Mustafa, A. Shah, C. Lewis, C. C. Tillman, T. Renduchintala, M. Li, S. Razmkhah, M. C. Hamilton, M. Annavaram, **S. Köse, and M. Pedram**, "System-Level Comparison of Superconductor-Semiconductor Interface Circuits," *IEEE Transactions on Applied Superconductivity*, Vol. 36, No. 5, pp. 1300507, August 2026.

J7. A. Adedokun, Y. Mustafa, and **S. Köse**, "Compromising qubit control in quantum computing via hardware Trojans in multitone generators," *Quantum Science and Technology*, Vol. 11, No. 2, March 2026.

J8. A. Y. Salim, B. Selman, H. Kautz, Z. Ignjatovic, and **S. Köse**, "SKI-SAT: A CMOS-compatible Hardware for Solving SAT Problems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 72, No. 10, pp. 5926 - 5937, October 2025.

J9. A. Adedokun, Y. Mustafa, and **S. Köse**, "Hardware Trojans in Superconducting Electronic Circuits," *Superconductor Science and Technology*, Vol. 38, No. 7, July 2025.

J10. E. Elmitwalli, Z. Ignjatovic, and **S. Köse**, "Constraint-aware Annealing for CMOS-based Ising Machine LPDC Decoder," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 72, No. 3, pp. 479 - 483, March 2025.

J11. Y. Mustafa and **S. Köse**, "Ternary Digital Output Data Link from SFQ Circuits," *IEEE Transactions on Applied Superconductivity*, Vol. 35, No. 5, pp. 1300405, August 2025.

J12. K. Krause, Y. Mustafa, A Shah, **S. Köse**, and M. C. Hamilton, "Signal Integrity Simulations of 4JL Gate Pulses from 4 K to 50 K," *IEEE Transactions on Applied Superconductivity*, Vol. 35, No. 5, pp. 1300506, August 2025.

J13. N. N. Anandakumar, M. Janke, J. Knechtel, X. Zhao, K. -S. Chong, **S. Köse**, B. -H. Gwee, J. Chang, L. Paul, and Y. Wang, "Hardware Security Attack Landscape and Countermeasures," *Hardware Security Attack Landscape and Countermeasures*, pp. 1 – 31, November 2024.

J14. S. Seçkiner and **S. Köse**, "A Methodology to Distribute On-Chip Voltage Regulators to Improve the Security of Hardware Masking," *Information*, Vol. 15, No. 8, pp. 1 – 12, August 2024.

J15. Y. Mustafa, K. Krause, A. Shah, M. C. Hamilton, and **S. Köse**, "DC-biased Suzuki Stack Circuit for Josephson-CMOS Memory Applications," *Superconductor Science and Technology*, Vol. 37, No. 8, pp. 085023, July 2024.

J16. Y. Mustafa and **S. Köse**, "Built-in Self-test of SFQ Circuits Using Side-channel Leakage Information," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 32, No. 6, pp. 1100–1109, June 2024.

J17. W. Liu, J Cheng, N. Sun, H. Sha, M. Jin, H. Zhao, Z. Pan, J. Wang, **S. Köse** and W. Yu, "A Low-Overhead and High-reliability Physical Unclonable Function (PUF) for Cryptography," *Integration*, Vol. 96, February 2024.

J18. N. Sun, W. Liu, J. Cheng, Z. Peng, C. Wang, C. Sun, H. Sha, Z. Pan, M. Jin, H. Zhao, J. Wang, Y. Wen, P. Kong, Y. Zhao, Y. Wang, **S. Köse**, and W. Yu, "A Novel SM4 Cryptographic Architecture against Higher Order Power Analysis Attacks," *International Journal of Circuit Theory and Applications*, January 2024.

J19. E. Elmitwalli, Z. Ignjatovic, and **S. Köse**, "Utilizing Multi-Body Interactions in a CMOS-Based Ising Machine for LDPC Decoding," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 71, No. 1, pp. 40–50, January 2024.

J20. Y. Mustafa and **S. Köse**, "Side-Channel Leakage in SFQ Circuits and Related Attacks on Qubit Control and Readout Systems," *IEEE Transactions on Applied Superconductivity*, Vol. 33, No. 6, pp. 1304307, September 2023.

J21. E. Elmitwalli and **S. Köse**, "Bistable Josephson Junction based True Random Number Generator without Inductors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 70, No. 4, pp. 1615 - 1619, April 2023.

J22. Y. Mustafa and **S. Köse**, "Suzuki Stack Circuit with Differential Output," *IEEE Transactions on Applied Superconductivity*, Vol. 33, No. 2, pp. 1300306, March 2023.

J23. J. Cheng, N. Sun, W. Liu, Z. Peng, C. Wang, C. Sun, Y. Wang, Y. Bi, Y. Wen, H. Zhang, P. Zhang, **S. Köse**, and W. Yu, "Neural Network-Based Entropy: A New Metric for Evaluating Side-Channel Attacks," *Journal of Circuits, Systems and Computers*, Vol. 32, No. 3, February 2023.

J24. Y. Mustafa and **S. Köse**, "Optimization of Suzuki Stack Circuit to Reduce Power Dissipation," *IEEE Transactions on Applied Superconductivity*, Vol. 32, No. 8, pp. 1 - 7, November 2022.

J25. S. Seçkiner and **S. Köse**, "Exploiting On-chip Voltage Regulators for Leakage Reduction in Hardware Masking," *Sensors*, Vol. 22, No. 18, pp. 1 – 25, September 2022.

J26. E. Elmitwalli, K. Ni, and **S. Köse**, "Machine Learning Attack Resistant Area-Efficient Reconfigurable Ising-PUF," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 30, No. 4, pp. 526 - 538, April 2022.

J27. Y. Mustafa, T. Jabbari, and **S. Köse**, "Emerging Attacks on Logic Locking in SFQ Circuits and Related Countermeasures," *IEEE Transactions on Applied Superconductivity*, Vol. 32, No. 3, pp. 1 - 8, March 2022.

J28. S. Seçkiner and **S. Köse**, "Preprocessing of the Physical Leakage Information to Combine Side-Channel Distinguishers," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 29, No. 12, pp. 2052 - 2063, December 2021.

J29. E. Elmitwalli, K. Ni, and **S. Köse**, "A PVT Tolerant True Random Number Generator based on Oscillator Phase under Sub-Harmonic Injection Locking," *IEEE Access*, Vol. 9, pp. 141626 - 141634, October 2021.

J30. F. Amsaad, A. Oun, M. Y. Niamat, A. Razaque, **S. Köse**, M. Mahmoud, W. Alasmary, and F. Alsolami, "Enhancing the Performance of Lightweight Configurable PUF for Robust IoT Hardware-Assisted Security," *IEEE Access*, Vol. 9, No. , pp. 136792 – 136810, October 2021.

J31. F. Amsaad and **S. Köse**, "A Secure Lightweight Hardware-assisted Charging Coordination Authentication Framework for Trusted Smart Grid Energy Storage Units," *Springer Nature - Computer Science*, pp. 1 – 15, September 2021.

J32. F. Amsaad and **S. Köse**, "A Secure Hardware-Assisted AMI Authentication Scheme for Smart Cities," *IEEE Consumer Electronics Magazine*, Vol. 10, No. 4, pp. 106 – 112, July 2021.

J33. B. Peköz, M. Hafez, **S. Köse** and H. Arslan, "Reducing Precoder/Channel Mismatch and Enhancing Secrecy in Practical MIMO Systems Using Artificial Signals," *IEEE Communications Letters*, Vol. 24, No. 6, pp. 1347 – 1350, June 2020.

J34. B. Peköz, **S. Köse** and H. Arslan, "Extensionless Adaptive Transmitter and Receiver Windowing of Beyond 5G Frames," *IEEE Transactions on Vehicular Technology*, Vol. 69, No. 2, pp. 1888 – 1902, February 2020.

J35. B. Peköz, Z. E. Ankaralı, **S. Köse** and H. Arslan, "Non-Redundant OFDM Receiver Windowing for 5G Frames and Beyond," *IEEE Transactions on Vehicular Technology*, Vol. 69, No. 1, pp. 676 – 684, January 2020.

J36. R. Kuttappa, **S. Köse** and B. Taskin, "FOPAC: Flexible On-Chip Power and Clock," *EEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 66, No. 12, pp. 4628 – 4636, December 2019.

J37. A. F. Demir, B. Peköz, **S. Köse** and H. Arslan,, "Innovative Telecommunications Training through Flexible Radio Platforms," *EEE Communications Magazine*, Vol. 57, No. 11, pp. 27 – 33, November 2019.

J38. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse** , " Exploring On-Chip Power Delivery Network Induced Analog Covert Channels," *IEEE TC on Cyber-Physical Systems Newsletter*, Vol. 4, No. 1, pp. 15 – 18, February 2019.

J39. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse** , "Exploiting Algorithmic Noise Tolerance for Scalable On-Chip Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, No. 1, pp. 229 – 242, January 2019.

J40. S. K. Khatamifard, L. Wang, **S. Köse**, and U. R. Karpuzcu, "A New Class of Covert Channels Exploiting Power Management Vulnerabilities," *IEEE Computer Architecture Letters (CAL)*, Vol. 17, No. 2, pp. 201 – 204, July-December 2018.

J41. W. Yu, Y. Chen, **S. Köse**, and J. Chen, "Exploiting Multi-Phase On-Chip Voltage Regulators as Strong PUF Primitives for Securing IoT," *Journal of Electronic Testing*, Vol. 34, No. 5, pp. 587 – 598, October 2018.

J42. M. Azhar, F. Amsaad, and **S. Köse**, "Duty Cycle-based Controlled Physical Unclonable Function," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 26, No. 9, pp. 1647 – 1658, September 2018.

J43. F. Amsaad, M. Niamat, A. Dawoud, and **S. Köse**, "Reliable Delay based Algorithm to Boost PUF Security against Modeling Attacks," *Information*, Vol. 9, No. 9, pp. 1 – 15, September 2018.

J44. W. Yu and **S. Köse**, "Exploiting Voltage Regulators to Enhance Various Power Attack Countermeasures," *IEEE Transactions on Emerging Topics in Computing*, Vol. 6, No. 2, pp. 244 – 257, April-June 2018.

J45. S. A. Sadat, M. Canbolat, and **S. Köse**, "Optimal Allocation of LDOs and Decoupling Capacitors within a Distributed On-Chip Power Grid," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol 23, No. 4, pp. 49:1 – 49:15, May 2018.

J46. M. H. Yilmaz, E. Guvenkaya, H. M. Furqan, **S. Köse**, and H. Arslan , "Cognitive Security of Wireless Communication Systems in the Physical Layer," *Wireless Communications and Mobile Computing*, Vol. 2017, pp. 1 – 9, December 2017.

J47. M. H. Yilmaz, **S. Köse**, N. Chamok, M. Ali, and H. Arslan , "Partially Overlapping Filtered Multitone with Reconfigurable Antennas in Uncoordinated Networks," *Physical Communication*, Vol. 25, No. 1, pp. 249 – 258, December 2017.

J48. W. Yu and **S. Köse**, "False Key-Controlled Aggressive Voltage Scaling: A Countermeasure Against LPA Attacks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 36, No. 12, pp. 2149 – 2153, December 2017.

J49. L. Wang, S. K. Khatamifard, O. A. Uzun, U. R. Karpuzcu, and **S. Köse** , "Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing among Distributed On-Chip Voltage Regulators," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 11, pp. 3019 – 3032, November 2017 .

J50. W. Yu and **S. Köse**, "A Lightweight Masked AES Implementation for Securing IoT Against CPA Attacks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 64, No. 11, pp. 2934 – 2944, November 2017.

J51. W. Yu and **S. Köse**, "Security-Adaptive Voltage Conversion as a Lightweight Countermeasure Against LPA Attacks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 7, pp. 2183 - 2187, July 2017.

J52. W. Yu and **S. Köse**, "A Voltage Regulator-Assisted Lightweight AES Implementation Against DPA Attacks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 63, No. 8, pp. 1152 - 1163, August 2016.

J53. W. Yu and **S. Köse**, "Charge-Withheld Converter-Reshuffling (CoRe): A Countermeasure Against Power Analysis Attacks," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 63, No. 5, pp. 438 - 442, May 2016.

J54. W. Yu and **S. Köse**, "Security Implications of Simultaneous Dynamic and Leakage Power Analysis Attacks on Nanoscale Cryptographic Circuits," *IET Electronics Letters*, Vol. 52, Issue 6, pp. 466 - 468, March 2016.

– Featured as the *Interview* article of the March issue of the IET Electronics Letters.

J55. W. Yu and **S. Köse**, "Time-Delayed Converter-Reshuffling: An Efficient and Secure Power Delivery Architecture," *IEEE Embedded Systems Letters*, Vol. 7, No. 3, pp. 73 - 76, September 2015.

J56. I. Vaisband,B. Price, **S. Köse**, Y. Kolla, E. G. Friedman, and J. Fischer, "Distributed Power Delivery with 28 nm Ultra-Small LDO Regulator," *Analog Integrated Circuits and Signal Processing*, Vol. 83, Issue 3, pp. 295 - 309, March 2015.

J57. I. Vaisband, M. Azhar, E. G. Friedman and **S. Köse**, "Digitally Controlled Pulse Width Modulator for On-Chip Power Management," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 12, pp. 2527 - 2534, December 2014.

J58. O. Uzun and **S. Köse**, "Converter-Gating: A Power Efficient and Secure On-Chip Power Delivery System," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 4, No. 2, pp. 169 - 179, June 2014.

J59. **S. Köse**, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active Filter Based Hybrid On-Chip DC-DC Converters for Point-of-Load Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 21, No. 4, pp. 680 - 691, April 2013.

J60. I. Savidis, **S. Köse**, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 2, pp. 587 - 597, February 2013.

J61. **S. Köse** and E. G. Friedman, "Distributed On-Chip Power Delivery," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 4, No. 4, pp. 704 - 713, December 2012.

J62. **S. Köse** and E. G. Friedman, "Efficient Algorithms for Fast IR Drop Analysis Exploiting Locality," *Integration, the VLSI Journal*, Vol. 45, No. 2, pp. 149 - 161, March 2012.

J63. **S. Köse** and E. G. Friedman, "Effective Resistance of a Two Layer Mesh," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 58, No. 11, pp. 739 - 743, November 2011.

J64. **S. Köse**, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 8, pp. 1458 - 1468, August 2011.

Conferences

C1. R. Marsala, Y. Mustafa, P. Tangella, M. Sonji, G. Michelogiannakis, **S. Köse**, A. Jog, M. E. Belviranli, "Hibiscus: End-to-end Architectural Simulation Framework for Hybrid SFQ/CMOS-Memory Compute Systems," *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2026.

C2. A. Adedokun and **S. Köse**, "Cyclic QFP Network with Controllable Bistability for Scalable Superconducting Spin Systems," *IEEE International System-on-Chip Conference (SOCC)*, September 2025.

C3. Y. Mustafa and **S. Köse**, "Lightweight Error-Correction Code Encoders in Superconducting Electronic Systems," *IEEE International System-on-Chip Conference (SOCC)*, September 2025.

C4. A. Adedokun, Y. Mustafa, and **S. Köse**, "Bistable All-Josephson Junction SQUID with Dual Φ-Junctions for State-Controlled Superconducting Circuits," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2025.

C5. J. Wu, E. Elmitwalli, A. Y. Salim, **S. Köse**, and Z. Ignjatovic, "A Pseudo-Random Number Generator for Multi-Sequence Generation with Programmable Statistics," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2025.

C6. E. Elmitwalli, Z. Ignjatovic, and **S. Köse**, "CMOS Ring Oscillator Ising Machine Using Sub-Harmonic Injection Locking," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2025.

C7. Y. Mustafa and **S. Köse**, "S-PAM: Superconductor-Semiconductor Interface Circuit with Pulse-Amplitude Modulation," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2025.

C8. A. Adedokun, Y. Mustafa, and **S. Köse**, "Watermarking Superconducting Electronic Circuits in Classical and Quantum Computers," *IEEE Microelectronics Design and Test Symposium (MDTS)*, May 2025.

C9. I. Dagli, J. Crea, S. Seckiner, Y. Xu **S. Köse**, and M. E. Belviranli , "MC^3: Contention-based Covert Channels Exploiting Shared DRAM Vulnerabilities on System-on-Chips," *Proceedings of the IEEE Design, Automation and Test in Europe Conference and Exhibition (DATE)*, March 2025.

C10. A. Adedokun, Y. Mustafa, and **S. Köse**, "Trojan Threats in Quantum Computing Hardware: SFQ Control and Readout Vulnerabilities," *Proceedings of the IEEE Conference on Secure IoT, Assured and Trusted Computing (SATC)*, February 2025.

C11. Y. Mustafa and **S. Köse**, "Side-Channel Attacks Targeting Classical-Quantum Interface in Quantum Computers," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2024.

C12. Y. Mustafa and **S. Köse**, "Side-Channel Leakage in Superconductive Electronics: Foe or Friend?," *IEEE Microelectronics Design and Test Symposium (MDTS)*, May 2024.

C13. Y. Mustafa and **S. Köse**, "Covert Communication Attacks in Chiplet-based 2.5-D Integration Systems," *IEEE International System-on-Chip Conference (SOCC)*, September 2023.

C14. Y. Mustafa and **S. Köse**, "Modeling and Analysis of Switched-Capacitor Converters as a Multi-port Network for Covert Communication," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, June 2023.

C15. S. Seçkiner and **S. Köse**, "Security Implications of Decoupling Capacitors on Leakage Reduction in Hardware Masking," *Proceedings of the IEEE Latin America Symposium on Circuits and System (LASCAS)*, March 2023.

C16. Y. Mustafa and **S. Köse**, "Side-channel Leakage in Suzuki Stack Circuits," *International Symposium on Quantum Computing: Circuits Systems Automation and Applications (QC-CSAA)*, July 2022.

C17. S. Seçkiner and **S. Köse**, "Combined Side-Channel Attacks on a Lightweight Prince Cipher Implementation," *Proceedings of the IEEE International SoC Conference*, September 2021.

C18. F. Amsaad and **S. Köse**, "A Lightweight Hardware-Based Authentication for Secure Smart Grid Energy Storage Units," *IEEE World Forum of Internet of Things (WF-IoT)*, June 2021.

C19. F. Amsaad, A. Razaque, M. Baza, **S. Köse**, S. Bhatia and G. Srivastava, "An Efficient and Reliable Lightweight PUF for IoT-based Applications," *IEEE International Conference on Communications Workshops*, pp. 1 - 6 June 2021.

C20. H. Dai and **S. Köse**, "On the Vulnerability of Hardware Masking in Practical Implementations," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, June 2021.

C21. L. Wang and **S. Köse**, "Startup Aware Reliability Enhancement Controller for On-Chip Digital LDOs," *Government Microcircuit Applications and Critical Technology Conference*, March 2021.

C22. S. Seçkiner and **S. Köse**, "Combined Distinguishers to Improve the Preprocessing Efficiency of Physical Leakage Measurements in Side-Channel Attacks," *Government Microcircuit Applications and Critical Technology Conference*, March 2021.

C23. L. Wang and **S. Köse**, "Approximate Voltage Regulation for Energy Efficient Error Tolerable Applications," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2020.

C24. A. Khanna, E. Elmitwalli, S. Dutta, S. Deng, S. Datta, **S. Köse**, and K. Ni, "A Bias and Correlation Free True Random Number Generator Based on Quantized Oscillator Phase under Sub-Harmonic Injection Locking," *IEEE Symposia on VLSI Technology and Circuits*, June 2020.

C25. F. Amsaad and **S. Köse**, "A Trusted Authentication Scheme for IoT-Based Smart Grid Applications," *IEEE World Forum of Internet of Things (WF-IoT)*, April 2020.

C26. S. Seçkiner, L. Wang and **S. Köse**, "An NBTI-Aware Digital Low-Dropout Regulator with Adaptive Gain Scaling Control," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October 2019.

C27. L. Wang, R. Kuttappa, B. Taskin, and **S. Köse**, "Distributed Digital Low-Dropout Regulators with Phase Interleaving for On-Chip Voltage Noise Mitigation," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2019.

C28. M. A. Vosoughi, L. Wang, and **S. Köse**, "Bus-Invert Coding as a Low-Power Countermeasure Against Correlation Power Analysis Attack," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2019.

C29. M. A. Vosoughi and **S. Köse**, "Combined Distinguishers to Enhance the Accuracy and Success of Side Channel Analysis," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019.

C30. M. A. Vosoughi and **S. Köse**, "Leveraging On-Chip Voltage Regulators Against Fault Injection Attacks," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, May 2019.

C31. L. Wang and **S. Köse**, "Reliability Enhanced On-Chip Digital LDO with Limit Cycle Oscillation Mitigation," *Government Microcircuit Applications and Critical Technology Conference*, March 2019.

C32. S. K. Khatamifard, L. Wang, A. Das, **S. Köse**, and U. R. Karpuzcu, "POWERT Channels: A Novel Class of Covert Communication Exploiting Power Management Vulnerabilities," *Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA)*, February 2019.

C33. L. Wang and **S. Köse**, "When Hardware Security Moves to the Edge and Fog," *Proceedings of the IEEE International Conference on Digital Signal Processing (DSP'18)*, November 2018.

C34. M. Azhar and **S. Köse**, "Process, Voltage, and Temperature-stable Adaptive Duty Cycle based PUF," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018.

C35. L. Wang and **S. Köse**, "Reliable On-Chip Voltage Regulation for Sustainable and Compact IoT and Heterogeneous Computing Systems," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, May 2018.

C36. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse**, "Mitigation of NBTI Induced Performance Degradation in On-Chip Digital LDOs," *Proceedings of the IEEE Design, Automation and Test in Europe Conference and Exhibition (DATE)*, pp. 803 - 808, March 2018.

C37. A. W. Khan, T. Wanchoo, G. Mumcu, and **S. Köse**, "Implications of Distributed On-Chip Power Delivery on EM Side-Channel Attacks," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, November 2017.

C38. B. Pekoz, **S. Köse**, and H. Arslan, "Adaptive Windowing of Insufficient CP for Joint Minimization of ISI and ACI Beyond 5G," *Proceedings of the IEEE Annual International Symposium on Personal, Indoor, and Mobile Radio Communications (PIMRC)*, October 2017.

C39. A. Roohi, R. Demara, L. Wang, and **S. Köse**, "Secure Intermittent-Robust Computation for Energy Harvesting Device Security and Outage Resilience," *Proceedings of the IEEE Conference on Advanced and Trusted Computing (ATC)*, August 2017.

C40. S. K. Khatamifard, L. Wang, W. Yu, **S. Köse**, and U. R. Karpuzcu, "ThermoGater: Thermally-Aware On-Chip Voltage Regulation," *Proceedings of the IEEE International Symposium on Computer Architecture (ISCA)*, pp. 120 - 132, June 2017.

C41. W. Yu and **S. Köse**, "A Lightweight AES Implementation Against Bivariate First-Order DPA Attacks," *Proceedings of the ACM Hardware and Architectural Support for Security and Privacy (HASP)*, pp. 1 - 7, June 2017.

C42. **S. Köse**, "Efficient and Secure On-Chip Reconfigurable Voltage Regulation for IoT Devices," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 369 - 374, May 2017.

C43. V. T. Alaparthy and **S. Köse**, "An Adaptive Senior Design Course with an Emphasis on Undergraduate Course Curriculum," *Proceedings of the IEEE International Conference on Microelectronics System Education*, pp. 59 - 62, May 2017.

C44. W. Yu and **S. Köse**, "Implications of Noise Insertion Mechanisms of Different Countermeasures Against Side-Channel Attacks," *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2017.

C45. **S. Köse**, L. Wang, and R. F. DeMara, "On-Chip Sensor Circle Distribution Technique for Real-Time Hardware Trojan Detection," *Government Microcircuit Applications and Critical Technology Conference (GOMACHTech)*, March 2017.

C46. W. Yu, O. A. Uzun, and **S. Köse**, "Leveraging On-Chip Voltage Regulators as a Countermeasure Against Side-Channel Attacks," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1 - 6, June 2015.

C47. M. E. Belviranli, W. Yu, and **S. Köse**, "Ultra-Fine Grain Power Management at Datapath-Level: Fact or Fiction," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) WACI Session*, March 2015.

C48. O. Uzun and **S. Köse**, "Regulator-Gating Methodology With Distributed Switched Capacitor Voltage Converters," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 13 - 18, July 2014.

C49. **S. Köse**, "Thermal Implications of On-Chip Voltage Regulation: Upcoming Challenges and Possible Solutions," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1 - 6, June 2014.

C50. M. Azhar and **S. Köse**, "An Enhanced Pulse Width Modulator with Adaptive Duty Cycle and Frequency Control," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 958 - 961, June 2014.

C51. **S. Köse**, "Regulator-Gating: Adaptive Management of On-Chip Voltage Regulators," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 105 - 110, May 2014.

C52. **S. Köse**, I. Vaisband, and E. G. Friedman, "Digitally Controlled Wide Range Pulse Width Modulator for on-Chip Power Supplies," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2251 - 2254, May 2013.

C53. **S. Köse**, R. M. Secareanu, O. Hartin, and E. G. Friedman, "Current Profile of a Microcontroller to Determine Electromagnetic Emissions" *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2650 - 2653, May 2013.

C54. **S. Köse** and E. G. Friedman, "Distributed Power Delivery for Energy Efficient and Low Power Systems," *Asilomar Conference on Signals, Systems, and Computers*, November 2012, **(invited paper)**.

C55. **S. Köse** and E. G. Friedman, "Design Methodology to Distribute On-Chip Power in Next Generation Integrated Circuits," *IEEE 27-th Convention of Electrical and Electronics Engineers in Israel*, November 2012, **(invited paper)**.

C56. **S. Köse** and E. G. Friedman, "Power Delivery in Heterogeneous Integrated Circuits," *IEEE CAS-FEST Workshop (in conjunction with ISCAS2012)*, May 2012, **(invited talk)**.

C57. **S. Köse**, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "An Area Efficient On-Chip Hybrid Voltage Regulator," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 398 - 403, March 2012.

C58. **S. Köse** and E. G. Friedman, "Fast Algorithms for IR Voltage Drop Analysis Exploiting Locality," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 996 - 1001, June 2011.

C59. **S. Köse** and E. G. Friedman, "Distributed Power Network Co-Design with On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2011.

C60. I. Savidis, **S. Köse**, and E. G. Friedman, "Power Grid Noise in TSV-Based 3-D Integrated Systems," *Government Microcircuit Applications and Critical Technology Conference (GOMACHTech)*, pp. 129 - 132, March 2011.

C61. **S. Köse** and E. G. Friedman, "Simultaneous Co-Design of Distributed On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the IEEE International SoC Conference*, pp. 15 - 18, September 2010.

C62. **S. Köse** and E. G. Friedman, "An Area Efficient Fully Monolithic Hybrid Voltage Regulator" *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2718 - 2721, May/June 2010.

C63. **S. Köse** and E. G. Friedman, "Fast Algorithms for Power Grid Analysis Based on Effective Resistance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 3661 - 3664, May/June 2010.

C64. **S. Köse** and E. G. Friedman, "On-Chip Point-of-Load Voltage Regulator for Distributed Power Supplies," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 377 - 380, May 2010.

C65. **S. Köse**, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2277 - 2280, May 2009.

C66. **S. Köse**, E. Salman, Z. Ignjatovic, and E. G. Friedman, "Pseudo-Random Clocking to Enhance Signal Integrity," *Proceedings of the IEEE International SoC Conference*, pp. 47 - 50, September 2008.

Patents

P1. Z. Ignjatovic, **S. Köse**, and A. Y. Salim "CMOS Competivle System and Method for Solving Boolean Satisfiability Problems," US Patent Application No. 63/633,922, April 15, 2024.

P2. Z. Ignjatovic, **S. Köse**, and E. Elmitwalli "System and Method for CMOS-based Decoding," US Patent Application No. 63/581,787, September 11, 2023.

P3. Z. Ignjatovic, **S. Köse**, and E. Elmitwalli "CMOS-based Ising Machine with Quantized States and Current-mode Coupling," US Patent Application No. 63/517,750, August 4, 2023.

P4. **S. Köse**, L. Wang, S. K. Khatamifard, and U. R. Karpuzcu, "Reduced Clock Pulse Width Digital Low-dropout Regulator," US Patent Application No. 17/410,896, February 2, 2022.

P5. **S. Köse**, L. Wang, S. K. Khatamifard, and U. R. Karpuzcu, "Method and apparatus for mitigating performance degradation in digital low-dropout voltage regulators (DLDOs) caused by limit cycle oscillation (LCO) and other factors," US Patent 11,573,586, February 7, 2023.

P6. L. Wang, S. K. Khatamifard, U. R. Karpuzcu, and **S. Köse**, "Method and apparatus for mitigating performance degradation in digital low-dropout voltage regulators (DLDOs)," US Patent 11,493,945, November 8, 2022.

P7. B. Taskin, R. Kuttappa, and **S. Köse**, "Flexible on-chip power and clock," US Patent 11,243,559, February 8, 2022.

P8. **S. Köse**, L. Wang, S. K. Khatamifard, and U. R. Karpuzcu, "Method and apparatus for mitigating performance degradation in digital low-dropout voltage regulators (DLDOs) caused by limit cycle oscillation (LCO) and other factors," US Patent 11,099,591, August 24, 2021.

P9. B. Pekoz, **S. Köse**, and H. Arslan, " System and method for extensionless adaptive transmitter and receiver windowing," US Patent 11,050,449, June 29, 2021.

P10. **S. Köse** and W. Yu, "False Key-controlled Aggressive Voltage Scaling," US Patent 10,873,446, December 22, 2020.

P11. **S. Köse** and W. Yu, "System and Method for Switched-Capacitor based Side-channel Countermeasures," US Patent 10,691,836, June 23, 2020.

P12. **S. Köse** and W. Yu, "Security-adaptive Voltage Conversion as a Lightweight Countermeasure against LPA Attacks," US Patent 10,680,797, June 9, 2020.

P13. B. Pekoz, M. Hafez, **S. Köse**, and H. Arslan, "Using artificial signals to maximize capacity and secrecy of multiple-input multiple-output (MIMO) communication," Us Patent 10,644,771, May 5, 2020.

P14. B. Pekoz, Z. E. Ankarali, **S. Köse**, and H. Arslan, "OFDM reception under high adjacent channel interference while preserving frame structure," US Patent 10,547,489, January 28, 2020.

P15. B. Pekoz, M. Hafez, **S. Köse**, and H. Arslan, "Using artificial signals to maximize capacity and secrecy of multiple-input multiple-output (MIMO) communication," Us Patent 10,516,452, December 24, 2019.

P16. B. Pekoz, **S. Köse**, and H. Arslan, "Network-Aware Adjacent Channel Interference Rejection and Out of Band Emission Suppression," US Patent 10,511,338, December 17, 2019.

P17. B. Pekoz, **S. Köse**, and H. Arslan, "Combined Minimization of Intersymbol Interference (ISI) and Adjacent Channel Interference (ACI)," US Patent 10,476,705, November 12, 2019.

P18. B. Pekoz, **S. Köse**, and H. Arslan, "Combined Minimization of Intersymbol Interference (ISI) and Adjacent Channel Interference (ACI)," US Patent 10,348,530, July 9, 2019.

P19. **S. Köse** and O. A. Uzun, "Secure Converter-Gating, Reconfiguration, and Regulation," US Patent 9,812,954, November 7, 2017.

P20. **S. Köse**, O. A. Uzun, and W. Yu, "Time Delayed Converter Reshuffling," US Patent 9,748,837, August 29, 2017.

P21. **S. Köse** and O. A. Uzun, "System and Method for Distributed Voltage Regulator-Gating," US Patent 9,372,490, June 21, 2016.

P22. **S. Köse** and E. G. Friedman, "A Digitally Controlled Wide Range Pulse Width Modulator," US Patent 9,007,140, April 14, 2015.

P23. **S. Köse** and O. A. Uzun, "System and Method for Voltage Regulator-Gating," US Patent 8,922,272, December 30, 2014.

Teaching

- **Instructor** University of Rochester
  Digital Logic (ECE112) Spring 2025, 40+ students
  Introduction to Hardware Security Fall 2024, 23 students
  Digital Logic (ECE112) Spring 2024, 45+ students
  Introduction to Hardware Security Fall 2023, 25 students
  Digital Logic (ECE112) Spring 2023, 45+ students
  Introduction to Hardware Security Fall 2022, 10 students
  Digital Logic (ECE112) Spring 2022, 40+ students
  Introduction to Hardware Security Fall 2021, 14 students
  Digital Logic (ECE112) Spring 2021, 40+ students
  Introduction to Hardware Security Fall 2020, 6 students
  Digital Logic (ECE112) Spring 2020, 40+ students
  Introduction to Hardware Security Fall 2019, 7 students
  Digital Logic (ECE112) Spring 2019, 80+ students

  University of South Florida
  Emerging Topics in Performance and Security of Modern Integrated Systems Spring 2017, 6 students
  Design II (Senior Design Project) Fall 2016, 40 students
  Design II (Senior Design Project) Spring 2016, 45 students
  Design II (Senior Design Project) Fall 2015, 40 students
  Design II (Senior Design Project) Spring 2015, 45 students
  Design II (Senior Design Project) Fall 2014, 40 students
  Design II (Senior Design Project) Spring 2014, 54 students
  High Performance Integrated Circuit Design Fall 2013, 8 students
  Introduction to Electrical Systems I (EGN 3373) Fall 2012, 120+ students

- **Co-Lecturer** University of Rochester
  Performance Issues in IC/VLSI Design and Analysis Fall 2011, 10+ students

- **Teaching Assistant** University of Rochester
  VLSI Design Methodologies Fall 2009, 10+ students
  Circuits and Signals Fall 2006, 30+ students
  Introduction to Signals and Circuits Spring 2007, 35+ students

- **Teaching Assistant** Bilkent University, Ankara
  Analog Electronics Fall 2004, Fall 2005, 100+ students
  Microprocessors Spring 2005, Spring 2006, 100+ students

Alumni

- **Soner Seckiner**, PhD, first job at Qualcomm 2025
- **Eslam Elmitwalli**, PhD, first job at Intel 2024
- **Berker Pekoz**, PhD, first job at Qualcomm 2020
- **Longfei Wang**, PhD, first job at Qualcomm 2018
- **Mahmood Azhar**, PhD, first job as Lead Instructor at South Florida State College 2018
- **Weize Yu**, PhD, first job as Assistant Professor at Old Dominion University 2017
- **Orhun Aras Uzun**, PhD, first job at Synaptics Corporation 2017
- **Rose McDonogh**, MSc, first job at Sandia National Labs 2022
- **Haotian Dai**, MSc, first job at PhD student at Rice University 2021
- **Ahmed Waheed Khan**, MSc, first job at Flex Electronics 2018
- **Tanya Wanchoo**, MSc, first job at Intel Corporation 2016

Current Graduate Students

- **Irem Zengin**, PhD student — Fall 2024 - present
- **Gulnur Kulzhanova**, PhD student — Fall 2024 - present
- **Ayisat Adedokun**, PhD student — Summer 2024 - present
- **Ahmet Yusuf Salim**, PhD student — Fall 2023 - present
- **Yerzhan Mustafa**, PhD student — Spring 2021 - present

Student Awards

- **Yerzhan Mustafa** — Cash Prize
  IEEE Council on Superconductivity Graduate Study Fellowship — *2024*
- **Longfei Wang** — Cash Prize
  Chih Foundation Research and Publication Award — *2018*
- **Longfei Wang** — Stipend+Tuition
  University of South Florida Graduate Fellowship — *2015 - 2016*
- **Weize Yu** — Stipend+Tuition+Travel
  University of South Florida Presidential Doctoral Fellowship — *2014 - 2019*

Professional Activities

- Associate editor
  IEEE Transactions on Circuits and Systems I: Regular Papers, 2023 – 2024
  Springer Nature - Computer Science, 2019 – present
  Microelectronics Journal, 2014 – present

- Committee member
  IEEE VLSI System Application Technical Committee, 2017 – present
  IEEE CASS Hardware Security Standards Committee, 2023 – present

- General chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2019

- Program co-chair
  IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024
  IEEE International Symposium on Smart Electronic Systems (iSES), 2021

- Technical track (co-)chair
  ACM/IEEE Design Automation Conference (DAC), 2022, 2023
  IEEE International System on Chip Conference (SOCC), 2019-2021
  ACM Great Lakes Symposium on VLSI (GLSVLSI), 2019-2021, 2023
  IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2018-2019

- Technical program committee member
  IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2021, 2023
  ACM/IEEE Design Automation Conference (DAC), 2020-2021
  IEEE Nordic Circuits and Systems Conference (NORCAS), 2019-2022
  IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2019
  IEEE International Symposium on Quality Electronic Design (ISQED), 2015-2021
  ACM Great Lakes Symposium on VLSI, 2013-2021
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2015-2021
  IEEE International Symposium on Circuits and Systems (ISCAS), 2017-2022
  IEEE Computer Society Annual Symposium on VLSI, 2014-2015

- Special session chair
  ACM Great Lakes Symposium on VLSI, 2022
  IEEE Computer Society Annual Symposium on VLSI, 2021

- Special session organizer
  Machine Learning Based Side Channel Attacks and Countermeasures at DAC'20
  Powering Heterogeneous IoT Systems: Design for Efficiency, Security, and Sustainability at GLSVLSI'18
  Efficient IoT Systems: The Power of Heterogeneous Integration at GLSVLSI'17

- Finance chair
  ACM Great Lakes Symposium on VLSI, 2019

- Tutorial chair
  IEEE International System on Chip Conference (SOCC), 2020-2021

- Student forum chair
  IEEE Computer Society Annual Symposium on VLSI, 2019

- Panel chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2018

- Publications chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2017

- Local arrangement chair
  IEEE Computer Society Annual Symposium on VLSI, 2014

- External reviewer
  Journals: *IEEE Journal of Solid-State Circuits (JSSC)*, *IEEE Transactions on Power Electronics (TPEL)*, *ACM Computing Surveys*, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits (TVLSI)*, *IEEE Transactions Circuits and Systems-I (TCAS-I)*, *IEEE Transactions Circuits and Systems-II (TCAS-II)*, *IEEE Transactions Computer-Aided Design (TCAD)*, *IEEE Electron Device Letters (EDL)*, *ASP Journal of Low Power Electronics (JOLPE)*, *Analog Integrated Circuits and Signal Processing*, *Integration, the VLSI Journal*, *IET Circuits, Devices & Systems*, *Microelectronics Journal*
  Conferences: International Conference on Computer-Aided Design (ICCAD), International Symposium on Quality Electronic Design (ISQED), Design, Automation and Test in Europa (DATE), International Conference on Circuits and Systems (ISCAS), International Conference on Computer Design (ICCD), System-on-Chip Conference (SOCC), Asia Pacific Conference on Circuits and Systems (APCCAS), International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), Asia Symposium on Quality Electronic Design (ASQED), International Symposium on Networks-on-Chip (NOCS), Great Lakes Symposium on VLSI (GLSVLSI), International Conference on Very Large Scale Integration (VLSI-SOC)

- Professional Societies
  Member, IEEE
  Member, ACM
  Member, NAI

Service

- Participant at the "CCC/SIGDA Workshop on Extreme Scale Design Automation" visioning workshop (invitation only), organized by ACM special interest group on design automation (ACM/SIGDA), 02/21-22/2014

- NSF Panelist, 2014, 2015, 2016, 2021, 2023, 2024, 2025, 2026